REFERENCE DRAWINGS - BUFFER LOGIC

CODE	DRAWING TITLE	DRAWING NO.
	Card Location and Listing	35216
01.[illegible].00	Interface Block Diagram	
02.[illegible].00	Memory Block Diagram	
03.[illegible].00	Vertical Format Block Diagram	
04.[illegible].00	Print Control Block Diagram	
01.01.01	On Line Control	
01.02.01	Load Control	
.03.01	Data Translator Control - A	
.03.02	Data Translator Control - B	
01.04.01	Data Translator	
01.05.01	Lamp Control	
01.06.01	Alarms	
.06.02	Set Alarms	
02.01.01	Odd Data Storage	
02.01.02	Even Data Storage	
.02.01	Data Write-Rewrite	
.02.02	Data Loads	
.03.01	Write Control	
.04.01	Preset Master Counter Units (1-6)	
.04.02	Preset Master Counter Units (7-0)	
.04.03	Preset Master Counter X00 thru X40	
.04.04	Preset Master Counter X50 thru X90	
02.05.01	Master Counter Units	
02.05.02	Master Counter C1-10 thru C81-90	
02.05.03	Master Counter C91-100 thru C121-130	
02.05.04	Master Counter C131-140 thru C151-160	
02.06.01	Memory Address "Units"	
02.06.02	Memory Address "Tens" & Hundreds	
03.01.01	Paper Feed Control	
.02.01	Vertical Format Control	
03.03.01	Vertical Format Channel Sel.	
04.01.01	Read Control	
04.01.02	Print Control	
.02.01	CW Storage	
.03.01	Compare Odd	
04.03.02	Compare Even	
04.04.01	B Register	
04.05.01	Enable Odd Column Gates	
04.05.02	Enable Even Column Gate	
04.06.01	C Register 6 thru 10	
04.06.02	C Register 1 thru 5	
04.07.01	Enable Zone Gates	
04.08.01	Test Generator Logic	
04.08.02	Test Data & Col. Counter	
	Schematic Magnetic Core Memory (2X-2Y-16X80)	

PRELIMINARY